Pergamon

Microelectron. Reliab., Vol. 36, No. 11/12, pp. 1735–1738, 1996

0026–2714/96 $15.00 + .00

PII: S0026–2714(96)00186–2

TURN-ON SPEED OF GROUNDED GATE NMOS ESD PROTECTION TRANSISTORS

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Abstract: The turn-on speed of nMOS transistors (nMOST) is of paramount importance for robust Charged Device Model (CDM) protection circuitry. In this paper the nMOST turn-on time has been measured for the first time in the sub-halve nanosecond range with a commercial e-beam tester. The method may be used to improve CDM-ESD hardness by investigating the CDM pulse responses within circuit. Furthermore it is shown that the CDM results of various protection layouts can be simulated with a SPICE model.

INTRODUCTION

In a highly automated IC production environment, the most relevant ESD hazards are represented by the fast discharge to ground of charge accumulated on a device through the manufacturing equipment. This ESD event is described by the Charged Device Model (CDM) and is characterised by durations and rise-times, in the nanosecond and sub-nanosecond range.

The availability of experimental techniques capable of characterising the response of protection circuits subjected to CDM ESD pulses is of crucial importance to improve IC hardness. In CMOS, ESD protection circuits usually employ grounded-gate nMOS transistors (gg-nMOST) as protection elements, because of their low on-resistance and satisfactory holding voltage (due to the parasitic bipolar transistor within their structure). With the introduction of the Charged Device Model [1], the question arises: *do most frequently applied ESD protection devices, gg-nMOSTs, trigger fast enough to provide adequate protection against CDM ESD hazards*? In recent years some experimental data on the turn-on time has been shown [2-4]. This paper will assess this question thoroughly through measurements and simulations of the turn-on time of gg-nMOSTs with variations of the main layout parameters. Because of the very fast sub-nanosecond transient and the inherent capacitive load of measurement probes, standard equipment is not capable of performing the transient measurements. Therefore, an electron beam testing system, with 150 ps time resolution has been used. In order to obtain a better insight of the experimental results, simulations have been carried out with a SPICE model.

EXPERIMENTAL RESULTS

Figure 1 shows a schematic sketch of the gg-nMOSTs under test with the variations of the main layout parameters: gate length (L), device width (W), drain-contact-to-gate spacing (DCGS) and source-contact-to-gate spacing (SCGS). It has been recently reported [3] that there is a remarkable influence of the gg-nMOST layout dimensions on the CDM performance.

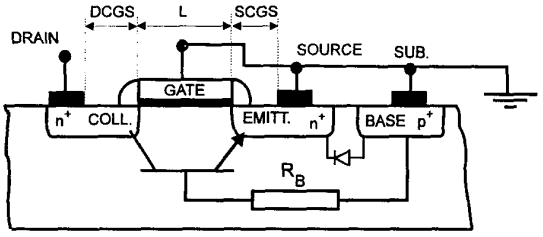

Figure 1 Basic ESD protection structure of the gg-nMOST showing the parasitic bipolar transistor and the main layout parameters.

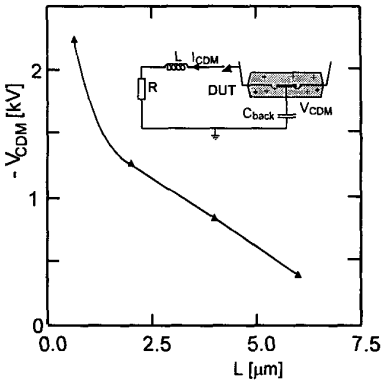

Figure 2 sCDM failure threshold for gg-nMOST (each measurements point resembles three devices).

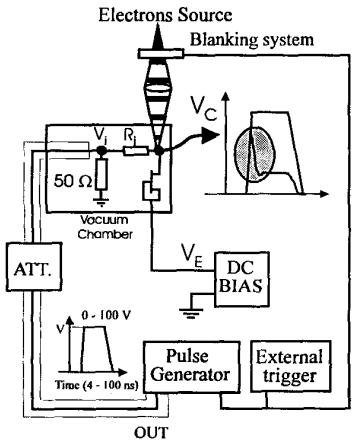

Figure 3 Schematic of the e-beam measurement set-up.

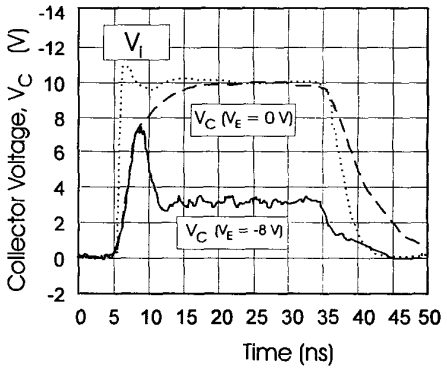

Figure 4 Typical transient measurements obtained with an E-Beam testing system. V_i is the voltage applied, V_c the voltage measured.

In Figure 2 the socketed CDM (sCDM) failure voltage threshold is shown as a function of the gg-nMOST gate length. There is a clear discrepancy between the smallest (0.5 μm) and larger gate length (2,4,6 μm) gg-nMOSTs concerning their capability to sustain the ultra-fast, high current CDM stress. Failure analysis revealed that devices with larger gate length (L > 2 μm) did not turn on completely during the CDM pulse and failed to clamp the applied voltage to a sufficiently low value [5]. This suggests that it is of great interest to carry out measurements on the turn-on time of these devices in order to have information about their applicability in CDM protection circuits.

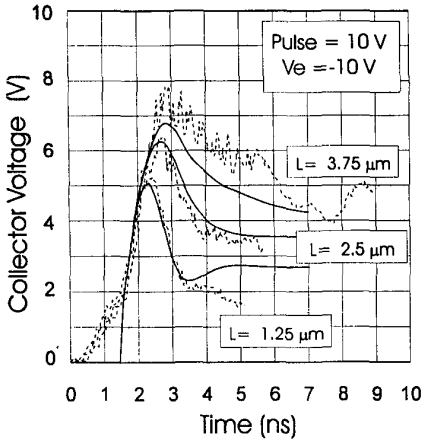

Figure 5 Turn-on measurements (dotted line) and simulation (continuous line) obtained on gg-nMOST with different values of gate length (L).

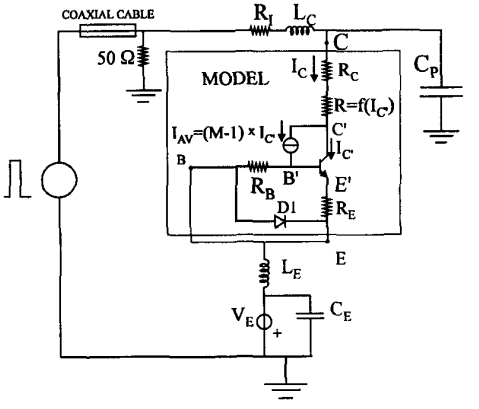

Figure 6 Equivalent circuit model for the SPICE simulations of triggering and turn-on.

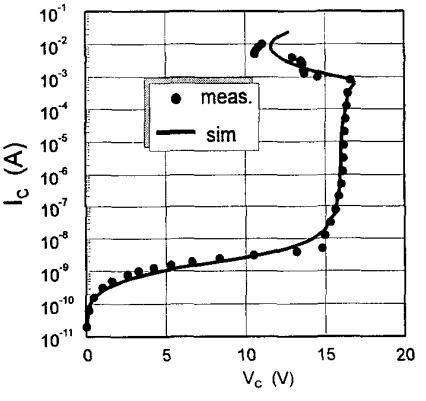

Figure 7 Measurements and simulation of the snap-back in a device with L=2.5 μm

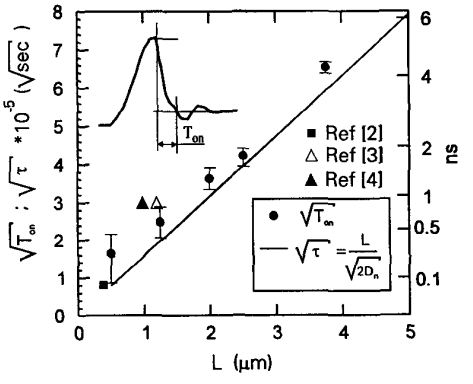

Figure 8 Turn-on time, T_{on}, and transit time, τ, of gg-nMOST as a function of the gate length, L, (i.e. base width of the npn BJT). In the picture is also depicted how T_{on} has been evaluated.

In Figure 3 a schematic of the e-beam measurement set-up is depicted. The emitter (source) and the base (substrate) of the gg-nMOST have been biased to -10 V in order to shift the signal measurement range from 0 V ÷ 20 V to -10 V ÷ 10 V. A 200 ps rise time pulse generator was used to apply short, fast rise time and high amplitude pulses, which are relevant to CDM hazard conditions. A typical turn on measurement is shown in Figure 4. When the drain to source voltage, Vds (or collector to emitter voltage Vce), becomes 16 V, the parasitic bipolar transistor (BJT) is triggered and Vds drops to about 11 V. The turn-on transient of the bipolar transistor is the key-point: it must be fast enough to fulfil the protection function during the 1-3 ns duration of the CDM discharge. In Figure 5 the results of the transient measurements (dotted lines) for different gg-nMOST gate lengths are depicted. The smaller gate length devices respond more quickly to the pulse. This is due to the fact that the transit time of the electrons in the base of the bipolar transistor is shorter and as such the turn-on becomes faster [6].

A SPICE model was developed, by adopting the transit times derived from e-beam measurements, extracting dc parameters and capacitances by means of IC-CAP and modelling impact-ionisation effects with a generator connected between base and collector and a simplified hydrodynamic model of the multiplication factor [7], see Figure 6. The derived model describes very accurately both transient (continuous line of Figure 5) and dc (Figure 7) electrical characteristics of grounded gate nMOST protection structures. In Figure 8 the response time, Ton and the theoretical transit time as a function of the gate length is shown. Only the gate length has a big influence on the Ton whereas the dependence on the DCGS and SCGS spacing has been found to be very small.

CONCLUSIONS

Measurements and simulations show that the most relevant parameter, concerning T_{on} in gg-nMOST protection devices, under CDM stress, is the gate length (parasitic npn base width). To ensure triggering under CDM conditions the gate length should be as short as possible in order to decrease the base transit time. Other layout parameter are not influencing the response time. We have also demonstrated that a commercial e-beam system with 150 ps time resolution is sufficient to thoroughly characterise the turn-on characteristics of protection structures subjected to the very fast CDM ESD pulses; the analysis of voltage spikes injected inside the IC beyond the protection structure is possible thus, giving the possibility of analysing possible over-voltages applied to the internal circuitry. Finally, some guidelines concerning the design of ESD protection structures have been obtained, and the capability of grounded-gate nMOST to turn-on sufficiently fast to provide adequate protection against CDM pulses has been demonstrated.

ACKNOWLEDGEMENTS

The authors wish to thank Christian Russ, Koen Verhaege (IMEC, Leuven, Belgium), Enrico Zanoni (University of Padova, Italy) for fruitful discussions. This work have been partially supported by the European Comunity under the Human Capital and Mobility Program (SUSTAIN Network).

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